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FIG. 1
 (Prior Art)

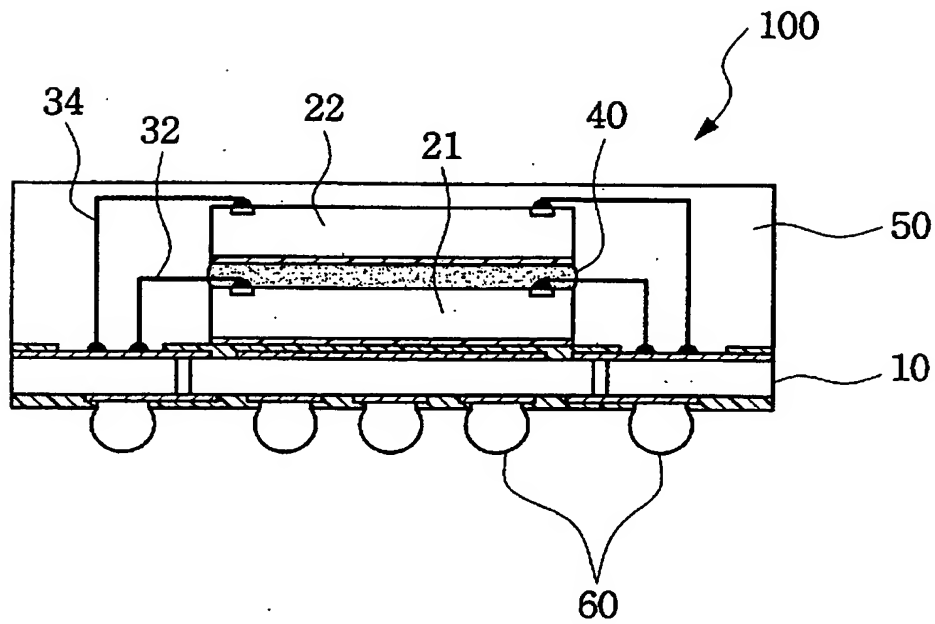
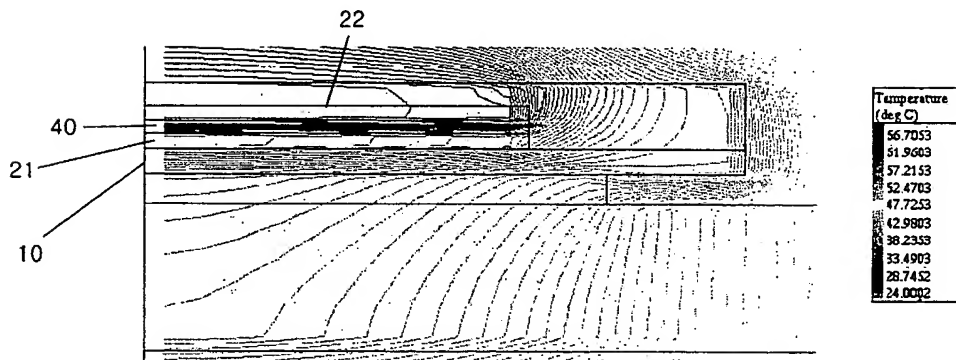


FIG. 2
 (Prior Art)



A cross-sectional view of a semiconductor device 200. The device features a substrate 110 with a top layer 111 and a bottom layer 112. A central region 114 is defined by a top layer 115 and a bottom layer 116. A central region 118 is defined by a top layer 119 and a bottom layer 120. A central region 121 is defined by a top layer 122 and a bottom layer 123. A central region 124 is defined by a top layer 125 and a bottom layer 126. A central region 127 is defined by a top layer 128 and a bottom layer 129. A central region 130 is defined by a top layer 131 and a bottom layer 132. A central region 133 is defined by a top layer 134 and a bottom layer 135. A central region 136 is defined by a top layer 137 and a bottom layer 138. A central region 139 is defined by a top layer 140 and a bottom layer 141. A central region 142 is defined by a top layer 143 and a bottom layer 144. A central region 145 is defined by a top layer 146 and a bottom layer 147. A central region 148 is defined by a top layer 149 and a bottom layer 150. A central region 151 is defined by a top layer 152 and a bottom layer 153. A central region 154 is defined by a top layer 155 and a bottom layer 156. A central region 157 is defined by a top layer 158 and a bottom layer 159. A central region 160 is defined by a top layer 161 and a bottom layer 162. A central region 163 is defined by a top layer 164 and a bottom layer 165. A central region 166 is defined by a top layer 167 and a bottom layer 168. A central region 169 is defined by a top layer 170 and a bottom layer 171. A central region 172 is defined by a top layer 173 and a bottom layer 174. A central region 175 is defined by a top layer 176 and a bottom layer 177. A central region 178 is defined by a top layer 179 and a bottom layer 180. A central region 181 is defined by a top layer 182 and a bottom layer 183. A central region 184 is defined by a top layer 185 and a bottom layer 186. A central region 187 is defined by a top layer 188 and a bottom layer 189. A central region 190 is defined by a top layer 191 and a bottom layer 192. A central region 193 is defined by a top layer 194 and a bottom layer 195. A central region 196 is defined by a top layer 197 and a bottom layer 198. A central region 199 is defined by a top layer 200 and a bottom layer 201.

A cross-sectional view of a semiconductor device 200. The device features a substrate 110 with a series of solder bumps 115a and 116a on its bottom surface. A base layer 112 is formed on the top surface of the substrate. A central component 120 is mounted on the base layer 112, consisting of a core 121, a top layer 122, and a bottom layer 127. A conductive layer 128 is positioned between the core 121 and the bottom layer 127. A layer 140 is located between the base layer 112 and the central component 120. A layer 136 is formed on the top surface of the base layer 112, surrounding the central component 120. A layer 150 is formed on the top surface of the layer 136. A layer 160 is formed on the bottom surface of the substrate 110, and a layer 160a is formed on the bottom surface of the layer 160.

The diagram illustrates a display device 300. It features a grid of pixels 211a. A set of horizontal control lines 211 is on the left, and a set of vertical control lines 221 is at the bottom. A central region contains a grid of pixels 211a. To the right, there are additional control lines 223a and 227a. A set of control lines 232 is on the left, and a set of control lines 236 is at the top. The entire display area is enclosed in a frame 210.

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FIG. 7

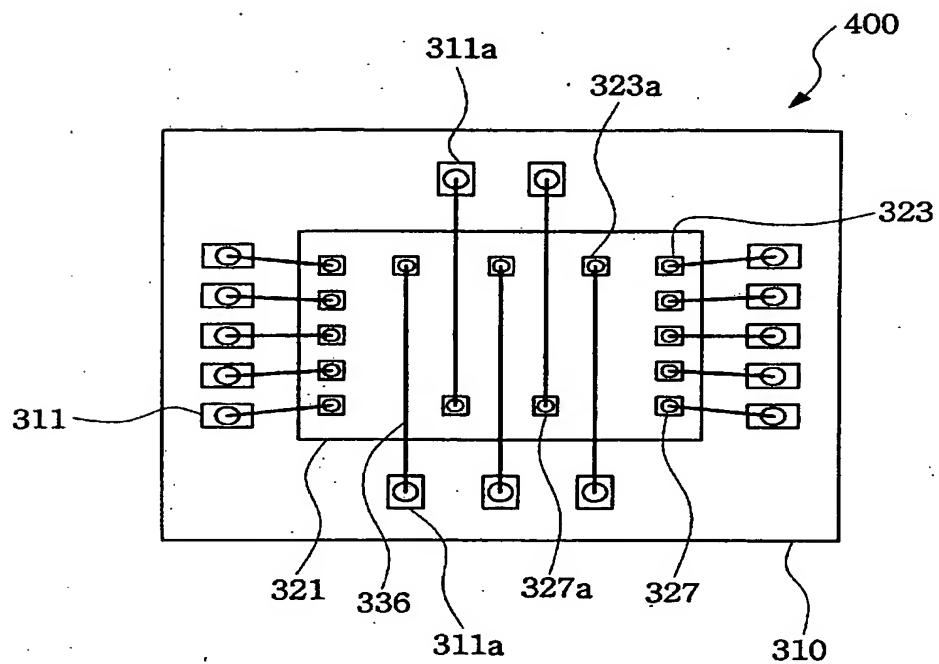


FIG. 8

